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nvSRAM – the non-volatile SRAM memory

Memories are essential elements of today's consumer electronics devices. These could be volatile versions (SRAM, DRAM), that are losing contents when switched off, and non volatile versions, that could retain data when power loss (EEPROM, FLASH). Combination of the two technologies can provide the advantage of fast memory solution with non-volatility. One of the possible choice is the nvSRAM technology, that we will introduce in this article based on the solutions provided by ANVO-Systems.

General features

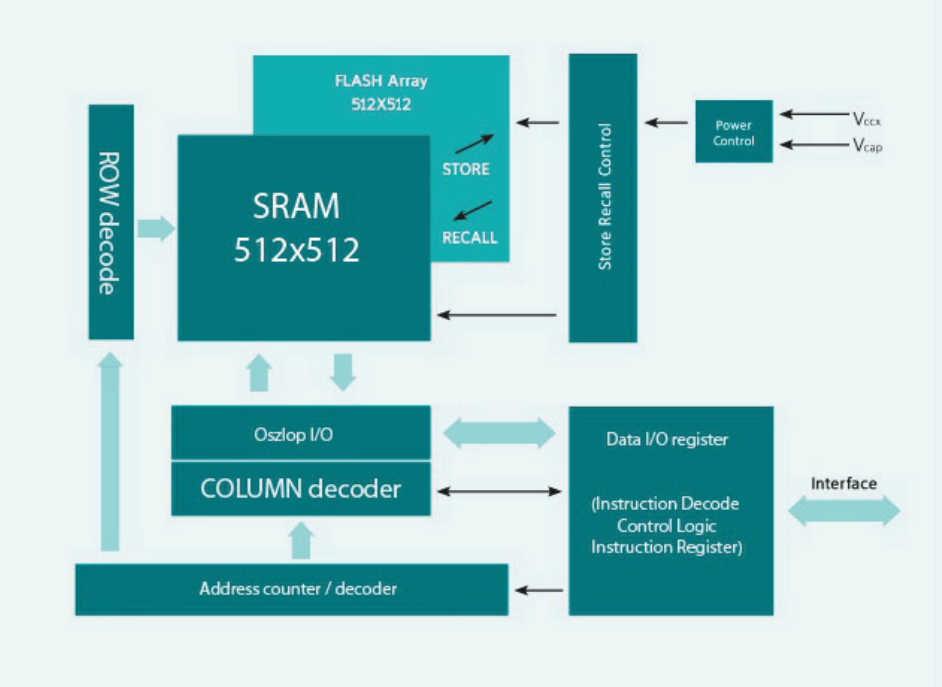
The non-volatile SRAMs from Anvo-Systems combine two technologies, CMOS-SRAM and SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) non-volatile memory into a new technology that has better features than the two standalone technics together.

The internal full SRAM functionality provides fast reads and writes executed with the same high speed, featuring however a built in data protection as well. The internal architecture of combining the SRAM array and the FLASH array, and the energy efficient STORE mechanism enable the device to transfer the whole SRAM data to/from the non-volatile array in just one single step operation (8ms STORE/10µs RECALL).

Since there is no wear out mechanism for write access the number of write cycles is unlimited and continuous write is possible. Besides storing the SRAM data to the Flash area during normal operation, the device can also execute a store operation on a power drop or at power down as well.

Operation

From the external circuit the nvSRAM looks like a normal SRAM, processor or



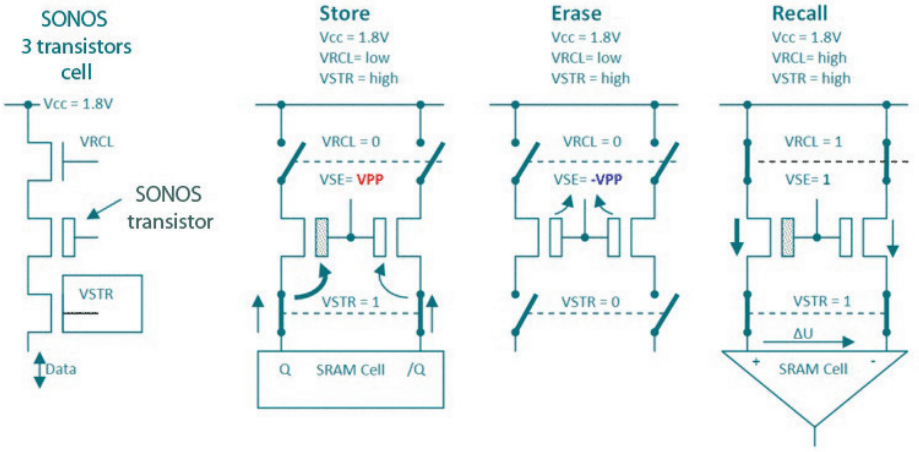
the controller could communicate with it via SPI or parallel interface.

However while SRAM can only read and write, the nvSRAM can read, write, store and recall.

Store and recall functions are used internally, between the SRAM array and the non-volatile Flash array.

When system power is on an internal reset command is executed. The backup capacitor starts charging. The SRAM and the FLASH cells are arranged side by side. When the power switches “on”, the RECALL command copies the contents of the non-volatile cells to the SRAM cells, the system is ready for external access, reading or writing the SRAM cells via the SPI or parallel interface.

If software command is forcing a STORE command, the contents of the SRAM cells are automatically copied into the Flash cells powered by the external power source Vcc (SOFTSTORE). When this power is lost an internal STORE command is executed automatically (AUTOSTORE) similar to the SOFTSTORE, but powered by one of the backup capacitances (also called POWERSTORE), which could be either an external capacitor connected to the VCAP pin, the system’s capacitance or an internal capacitor. The STORE commands usually take 8 ms, which is comparable with an EEPROM or Flash write cycle. The RECALL function is powered by Vcc, therefore its time consumption is in the µs range.



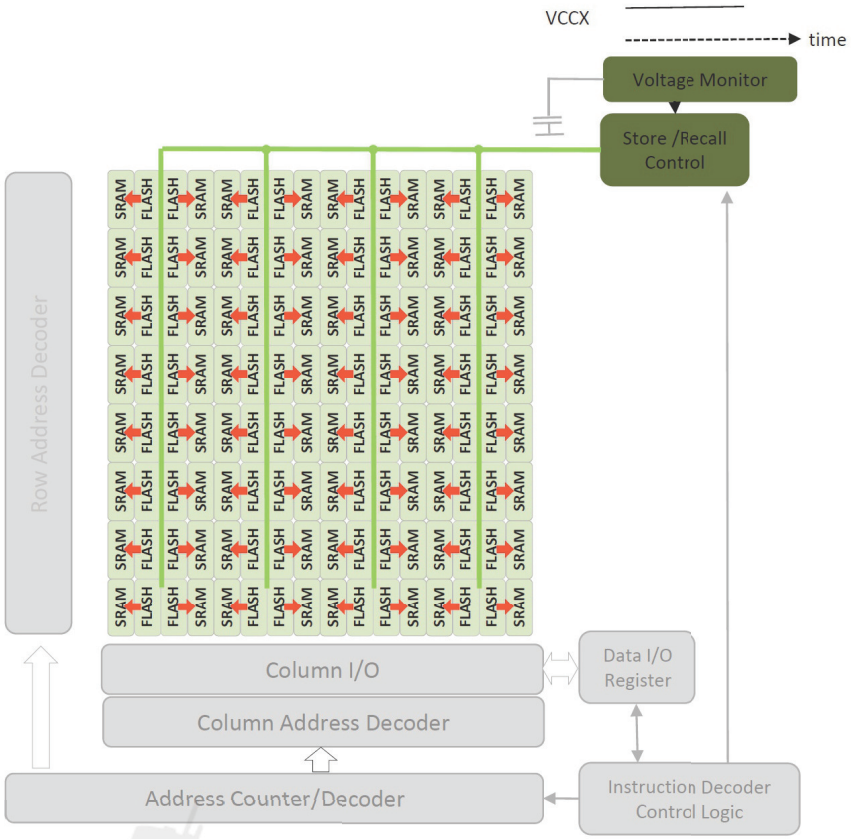
During the power is OFF, the nvSRAM works like a storage device, the Flash cells keep the data available without external power.

During operation the device acts as a fast SRAM, its speed is much higher than EEPROM or flash technology can provide. This is essential in heavily loaded microprocessor based data acquisition systems like metering applications. In order to have the data integrity even in harsh environments, ANVO Systems introduced the capability of secure read and write operations. The algorithm uses a checksum calculation on data transfer that has been evaluated before read or write is accepted. This makes sure that data integrity is not broken during storage.

Some of new features have been added by ANVO systems to the existing nvSRAM technology. Non-volatile logging of the last successful write operation improves system recovery. The differential memory cell – two storage element for each data bits – improve reliability, speed and stability. The page and block roll over option makes it possible to continuously writing on one 64bit page, while a free 2 Byte non-volatile register can be a solution for serial numbering.

Using of nvSRAM

The nvSRAM technology will provide data protection in case of sudden power failure and allow recall data without power consumption. It also takes the advantages that traditional SRAM can offer, like the high write speed, unlimited cycles, energy efficiency, non-destructive data read, wear proofness, and simple access protocol. The new ANVO memory solutions are especially suitable for applications such as smart metering, e-health, industrial control, home automation as well as sports and fitness.



The 100 year of non-volatile data retention makes the data safe forever. While first ANVO-Systems' nvSRAM solu-tions ICs were available with a serial SPI interface, now also parallel nvSRAM products with 25 nanosecond access time, unlimited read-/write cycles, several store options as well as unique security features are available.